Design of Efficient Sense Amplifier based Flip-flop using GDI Technique

Priyanka Sharma, Neha Arora, Prof. B. P .Singh

Abstract— Design of a new sense amplifier-based flip-flop (SAFF) using GDI Technique and performance comparison of proposed SAFF with existing conventional SAFF with CMOS-NAND latch SAFF and SAFF with CMOS Symmetric latch is presented in this paper. It was found that the main drawback of existing SAFF's is the cross-coupled set-reset (SR) latch in the output stage. The new flip-flop uses a new output stage latch topology using GDI that significantly reduces power consumption and has improved power-delay product (PDP). Different topologies have been compared with respect to the number of devices, power consumption, power-delay product, temperature sustainability in order to prove the superiority of proposed design over existing conventional CMOS-NAND design. The simulation has been carried out on Tanner EDA tool on BSIM3v3 90nm technology.

Index Terms— CMOS digital integrated circuits, flip-flops, GDI Technique, latch topology, low power, Power-Delay product, Power consumption, Symmetric latch , sense-amplifier, Tanner EDA.

1 INTRODUCTION

Traditional CMOS logic had been modified by various logic design techniques such as pass transistor logic. Basically in Pass-transistor logic (PTL) logic, control signals are applied to the gates of NMOS transistors whereas data signals are applied to the sources of these transistors. Pass-transistor logics are beneficial over traditional CMOS logics in terms of power, speed and number of transistors. But due to some critical problems encountered in PTL implementations, it did not proved very successful in low power design aspects. There are two major problems with PTL which made it less efficient in low power designs. They are a) the threshold drop across the single-channel pass transistors results in the reduced current drive and hence reduced speed at low supply voltages.

This is major drawback in context of low power design where faster operation at low voltages is desirable. b) Since high input voltage level at the regenerative inverters is not V_{DD}, the PMOS device in the inverter is not fully turned off, and hence direct-path static power dissipation could be significant. Low logic level swing problem has been sorted out by using PMOS as well as NMOS in Transmission Gate (TG) logic design.CPL and DPL suffers from static power consumption due to the low swing at the gates of the output inverters and large area due to the presence of PMOS transistors.

Another low power design technique known as Gate-Diffusion-Input (GDI) technique that reduced power consumption, propagation delay and area of digital circuits while maintaining low complexity of logic design is discussed in this paper. The GDI approach allows implementation of a wide range of complex logic functions using only two transistors.

2 SENSE AMPLIFIER BASED FLIP-FLOP

2.1 CIRCUIT OPERATION

In general, a flip-flop consists of two stages: a pulse generator (PG) and a slave latch (SL). The SAFF consists of the SA in the first stage and the slave set-reset (SR) latch in the second stage as shown in Fig. 1.Sense Amplifier based Flip-flop (SAFF) is a flip-flop where the SA stage provides a negative pulse on one of the inputs to the slave latch, depending whether the output is to be set or reset. It senses the true and complementary differential inputs. The SA stage produces monotonic transitions from one to zero logic level on one of the outputs, following the leading clock edge. . Any subsequent change of the data during the active clock interval will not affect the output of the SA. The SR latch captures the transition and holds the state until the next leading edge of the clock arrives. After the clock returns to inactive state, both outputs of the SA stage assume logic one value.

Therefore, the whole structure acts as a flip-flop. When CLK is at low logic level, nodes labeled SB and RB are precharged through small P1 and P4 PMOS transistors in Fig. 2.When SB and RB are at high logic level N3and N4 are kept on, charging their sources up to V_{DD}-V_{tN} because there is no path to ground due to the off state of the clocked transistor N6.Since either N1or N2 is on, the common node of N1, N2 and N6 is also precharged to V_{DD}-V_{tN}. The inputs are decoupled from the outputs of the SA forming the base for the flip-flop

operation of the circuit. This flip-flop has differential inputs and is suitable for use with differential and reduced swing logic.

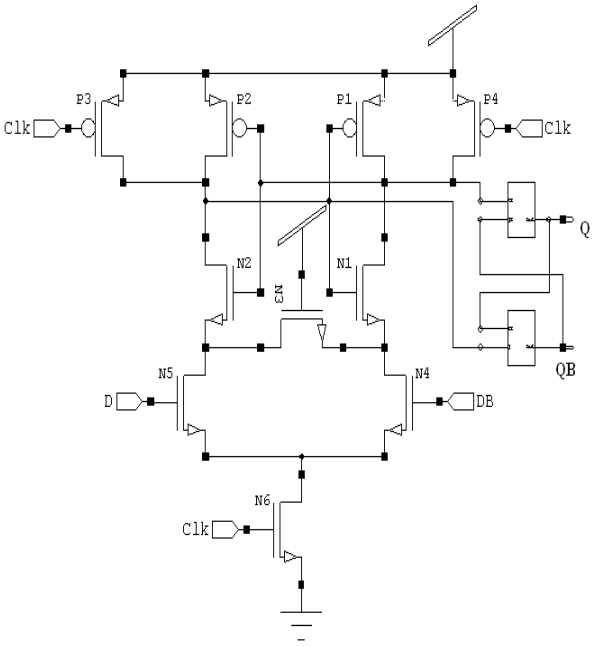

Fig. 1 Sense-Amplifier-based Flip-flop

2.2 SAFF TOPOLOGIES

2.2.1 CONVENTIONAL SAFF WITH CMOS-NAND LATCH DESIGN

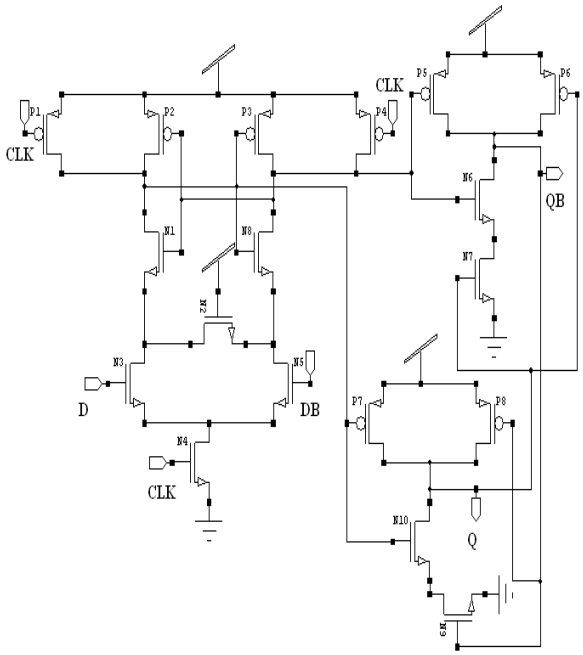

Fig. 2 SAFF with CMOS-NAND Latch Design

2.2.2 CONVENTIONAL SAFF WITH CMOS-SYMMETRIC LATCH

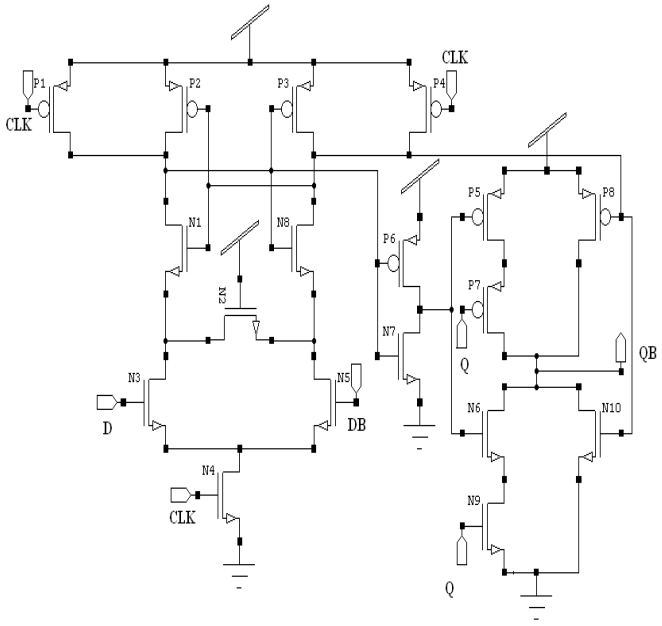

Fig. 3 SAFF with CMOS-Symmetric Latch

2.2.3 PROPOSED SAFF WITH LATCH USING GDI TECHNIQUE

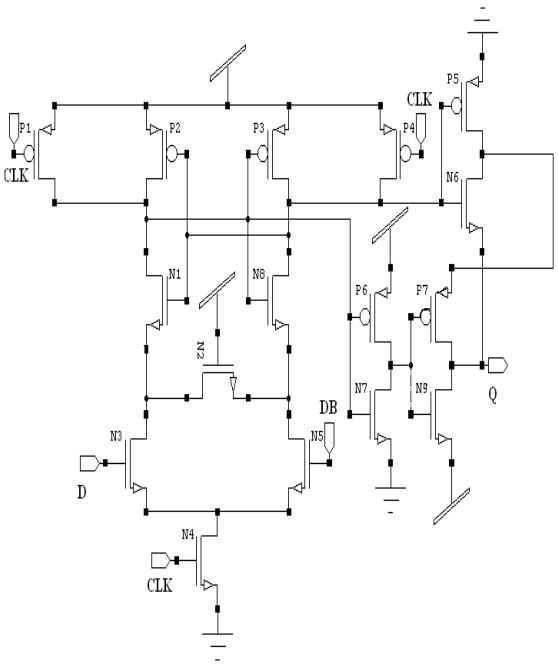

Fig.4 SAFF with latch using GDI Technique

3 Simulations and Analysis

3.1 Simulation Environment

All the circuits have been simulated using BISM 3V3 90nm technology on Tanner EDA tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns.

3.2 Simulation Comparison

In this section, proposed design using low power technique is consuming low power and has high performance as compared with SAFF with NAND-CMOS latch and SAFF with CMOS-Symmetric Latch in terms of power, delay and temperature at varying supply voltages. All the circuits have been simulated with supply voltage ranging .8 V to 1.6 V. Following graphs are shown between Power Consumption Vs Operating Temperature, Delay Vs V_{DD}, Power Consumption Vs V_{DD} for SAFF with NAND-CMOS latch, SAFF with CMOS-Symmetric Latch and SAFF with Latch using GDI technique respectively.Power consumption variation with different operating range of temperatures is shown at V_{DD}=1V.Following tables represent the quantitative approach showing the variation of power consumption for all the three topologies given above over different operating range of temperature, V_{DD}, and delay variation with V_{DD}. Finally, power-delay product comparison is shown in tabular form which reflects that our proposed circuit has least PDP and hence it is more efficient for low power VLSI designs.

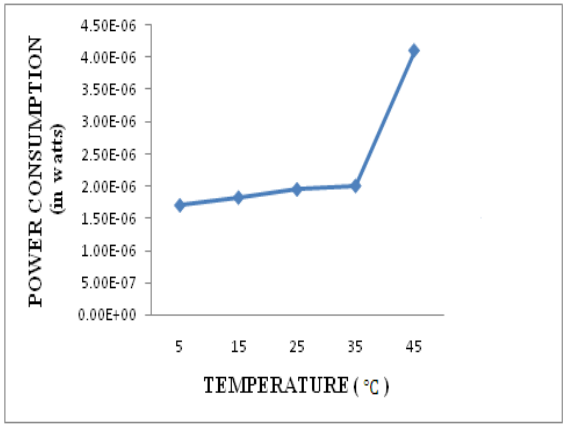

Fig. 5. Power consumption variation of SAFF with CMOS-NAND latch over different operating range of temperatures at V_{DD}=1V

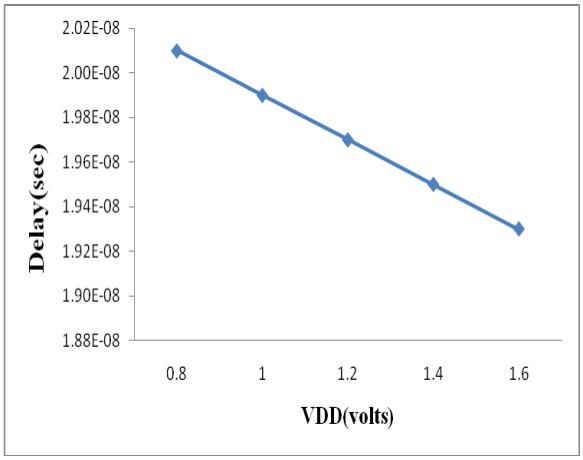

Fig. 6. Delay Variation of SAFF with CMOS-NAND latch over different operating range of V_{DD}

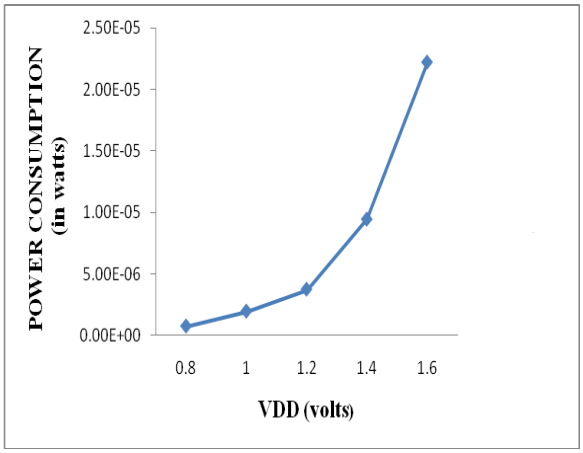

Fig. 7. Power consumption variation of SAFF with NAND CMOS latch with different operating range of V_{DD}

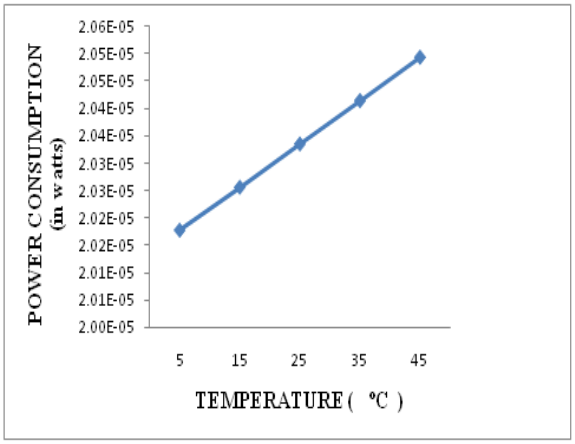

Fig. 8. Power consumption variation of SAFF with CMOS-Symmetric Latch with different operating range of temperatures at V_{DD}=1V

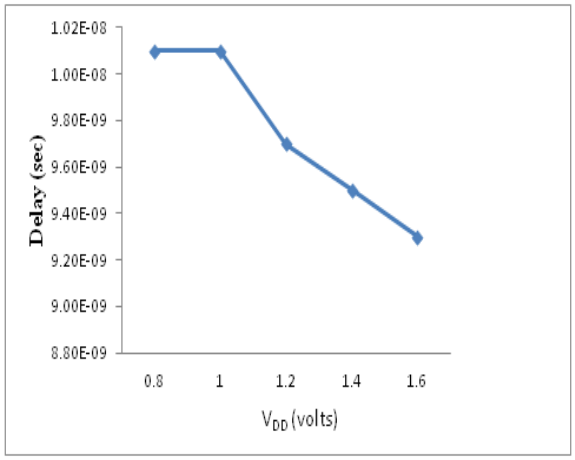

Fig. 9.Delay Variation of SAFF with CMOS-Symmetric Latch over different operating range of V_{DD}

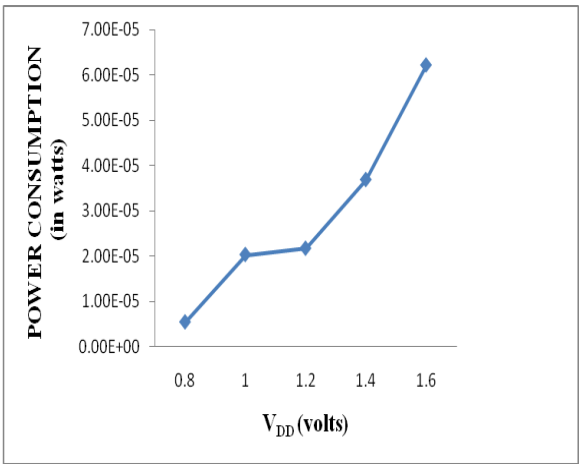

Fig. 10. Power consumption variation of SAFF with CMOS-Symmetric Latch with different operating range of V_{DD}

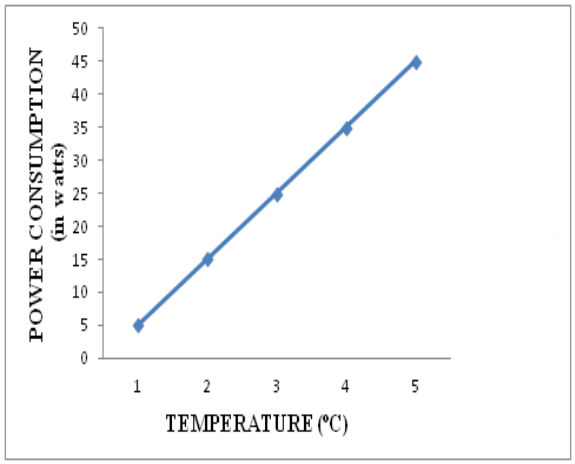

Fig. 11. Power consumption variation of SAFF with Latch using GDI technique with different operating range of temperatures at V_{DD}=1V

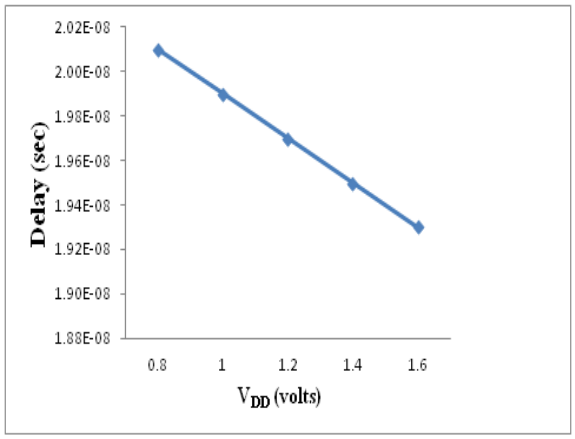

Fig.12. Delay Variation of SAFF with Latch using GDI technique over different operating range of V_{DD}

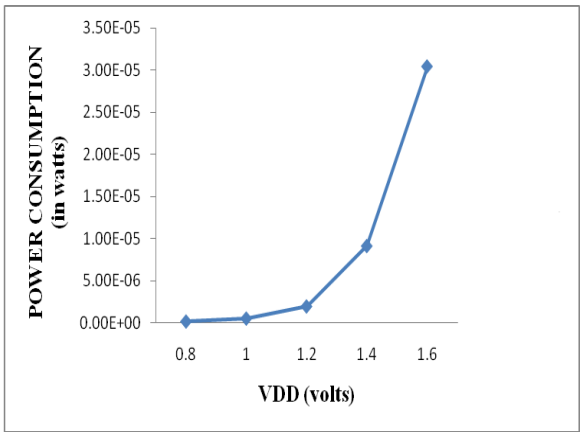

Fig. 13. Power consumption variation of SAFF with Latch using GDI technique over different operating range of V_{DD}

TABLE1
Power consumption variation of SAFF with CMOS-NAND latch over different operating range of temperatures at V_{DD}=1V

Temperature(°C)	Power consumption (in watts)
5	1.703004e-006
15	1.825101e-006
25	1.951543e-006
35	2.005288e-006
45	4.109265e-006

TABLE2
Delay Variation of SAFF with CMOS-NAND latch over different operating range of V_{DD}

V_{DD} (volts)	Delay (sec)
.8	2.0100e-008
1	1.9900e-008
1.2	1.9700e-008
1.4	1.9500e-008
1.6	1.9300e-008

TABLE 3
PDP of SAFF with CMOS-NAND latch at V_{DD}=1V

V_{DD}(volts)	PDP(volts-sec)
1	$3.3889*10^{-14}$

TABLE 4
Power consumption variation of SAFF with NAND CMOS latch over different operating range of V_{DD}

V_{DD} (volts)	Power consumption(in watts)
.8	7.440419e-007
1	1.951543e-006
1.2	3.737754e-006
1.4	9.428828e-006
1.6	2.219050e-005

TABLE 5
Power consumption variation of SAFF with CMOS-Symmetric Latch over different operating range of temperatures at V_{DD}=1V

Temperature(°C)	Power consumption (in watts)
5	2.017781e-005
15	2.025651e-005
25	2.033558e-005
35	2.041484e-005
45	2.049415e-005

TABLE 6
Delay Variation of SAFF with CMOS-Symmetric Latch over different operating range of V_{DD}

V_{DD} (volts)	Delay (sec)
.8	1.0100e-008
1	1.0100e-008
1.2	9.7000e-009
1.4	9.5000e-009
1.6	9.3000e-009

TABLE 7
Power consumption variation of SAFF with CMOS-Symmetric Latch over different operating range of V_{DD}

V_{DD} (volts)	Power consumption (in watts)
.8	5.448861e-006
1	2.033558e-005
1.2	2.172743e-005
1.4	3.689852e-005
1.6	6.221658e-005

TABLE 8
PDP of SAFF with CMOS-Symmetric Latch at V_{DD}=1V

V_{DD}(volts)	PDP(volts-sec)
1	$2.039*10^{-13}$

TABLE 9
Power consumption variation of SAFF with Latch using GDI technique over different operating range of temperatures at V_{DD}=1V

Temperature(°C)	Power consumption (in watts)
5	4.965438e-007
15	5.258306e-007
25	5.685602e-007
35	6.184802e-007
45	6.823192e-007

TABLE 10
Delay Variation of SAFF with Latch using GDI technique over different operating range of V_{DD}

V_{DD} (volts)	Delay (sec)
.8	2.0100e-008
1	1.9900e-008
1.2	1.9700e-008
1.4	1.9500e-008
1.6	1.9300e-008

TABLE 11
PDP of SAFF with Latch using GDI technique at V_{DD}=1V

V_{DD}(volts)	PDP(volts-sec)
1	$9.8704*10^{-15}$

TABLE 12
Power consumption variation of SAFF with Latch using GDI technique over different operating range of V_{DD}

V_{DD} (volts)	Power consumption (in watts)
.8	2.222364e-007
1	5.685602e-007
1.2	2.008319e-006
1.4	9.164612e-006
1.6	3.044173e-005

TABLE 13
PDP comparison of all three configurations given above

SAFF latch configurations	V_{DD}(volts)	PDP(volts-sec)	No. of transistors
NAND -CMOS	1	$3.388*10^{-14}$	18
CMOS-Symmetric	1	$2.039*10^{-13}$	18
GDI Technique	1	$9.870*10^{-15}$	16

4 CONCLUSION

This paper proposes a new design of SAFF with latch using GDI Technique, which resulted in better performance in terms of power consumption, number of transistors and, temperatures sustainability. The differential input signal nature of the flip-flop makes it compatible with the logic utilizing reduced signal swing.GDI Technique contributed in improved PDP of new design also. Hence, the proposed design can be used for other complex designs. All the simulations are carried out at Tanner EDA tool at BSIM3v3 90nm technology.

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